

CLAIMS

1. (Amended) A semiconductor device comprising:

5 a semiconductor chip;  
a protective package for covering the semiconductor chip, including at least a pair of opposed side surfaces, each of the side surfaces having a first slanted portion and a second slanted portion each being flat and meeting the other at a predetermined  
10 angle;

a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package;

15 a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package;

20 wherein the inner portions and the outer portions of the first and the second leads are flat, extending in a same plane,

wherein the outer portions of the first lead extend from both of the pair of opposed side surfaces out of the protective package, and

25 wherein the outer portions of the second lead extend from both of the pair of opposed side surfaces out of the protective package.

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5. (Amended) The semiconductor device according to Claim 1, wherein the outer portions of the first and the second leads extend out of the protective package, from places where the first slanted portion and the second slanted portion meet each other.

6. (Amended) The semiconductor device according to Claim 5, wherein the first slanted portion and the second slanted portion meet each other generally at a thickness-wise center of the protective package.

7. The semiconductor device according to Claim 1, wherein the semiconductor chip is a light emitting element.

8. The semiconductor device according to Claim 1, wherein the semiconductor chip is a light receiving element.

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9. (Deleted)

10. (Amended) A mounting structure of a semiconductor device on a circuit substrate,

the semiconductor device including: a semiconductor chip; a protective package for covering the semiconductor chip, including at least a pair of opposed side surfaces, each of the side surfaces having a first slanted portion and a second slanted portion each being flat and meeting the other at a predetermined angle; a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; the inner portions and the outer portions of the first and the second leads being flat and extending in a same plane; the outer portions of the first lead extending from both of the pair of opposed side surfaces out of the protective package; the outer portions of the second lead extending from both of the opposed side surfaces out of the protective package;

the circuit substrate including: a main surface formed with a predetermined wiring pattern; a plurality of connecting pads formed in the main surface; and a through hole corresponding to a shape of the protective

package;

wherein the protective package is fitted into the through hole and the outer portions of the first lead and the second lead are connected with the connecting

5 pads.

11. The mounting structure according to Claim 10, wherein the connecting pads are disposed around the through hole.

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12. The mounting structure according to Claim 10, wherein the main surface mounted with the semiconductor device is laminated with a coating member.

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17. (Added) A method for manufacturing a semiconductor device using a lead frame, the lead frame including a pair of side bars and a plurality of pairs of cross bars, each pair of the cross bars including a first cross bar bridging the pair of side bars and having an

intermediate portion formed with a bonding pad and a second cross bar bridging the pair of side bars near the first cross bar, the pair of side bars being interconnected only by the first and the second cross bars; the method comprising:

5 a semiconductor-chip bonding step of bonding a semiconductor chip to the bonding pad, establishing electrical connection with the first cross bar; a wire bonding step of electrically connecting the semiconductor chip with the second cross bar located near the first cross bar; and

10 a protective-package formation step of forming a protective package using a resin, for sealing the semiconductor chip, the wire, part of the first cross bar including the bonding pad, and part of the second cross bar including a portion connected with the wire.

15 18. (Added) The method according to Claim 17, wherein the lead frame is heated in the wire bonding step.